

1.1.1

STRUCTURE AND FUNCTION OF THE PROCESSOR

TOPIC WISE EXAM QUESTIONS

ANSWERS

A-LEVEL

OCR

4	(b)	(i)	<ul style="list-style-type: none"> Can execute multiple instructions / FDE cycles at the same time // some instructions in the program can be run in parallel 	1	<p>Do not accept just "multiple instructions"</p> <p>Do not accept tasks/programs for instructions</p>
4	(b)	(ii)	<ul style="list-style-type: none"> Some instructions may not be able to be run in parallel An instruction may be dependent / waiting for other instructions to be completed Other factors influence processing speed – clock speed / cache / bottlenecks / etc Program / OS needs to be written to specifically use multiple cores 	2	

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1	(a)	<ul style="list-style-type: none"> Clock Speed The speed at which the fetch decode execute cycle is completed/ the speed a single core can execute instructions Number of cores/ independent processing unitsthat can fetch decode execute at the same time Cache size... ... memory that contains recently/frequently used instructions/data ...memory that has a faster R/W speed than RAM ...memory that is closer to/onboard the CPU 	AO1.1 (2) AO1.2 (2)	<p>One mark for stating the factor, mark for expanding the factor</p> <p>- Accept cycles for "FDE Cycles"</p>
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1	(a)	(i)	<ul style="list-style-type: none"> Both <u>data and instructions</u> share the same memory <u>Instructions and Data</u> stored in same format A single set of buses / same <u>bus for instructions & data</u> (to connect CPU to Memory and I/O) Has a (single) control unit Has an ALU. Has ways to input and output. Has access to storage, Works sequentially through instructions // follows Fetch-execute cycle (Special) registers within CPU Based on stored program concept 	2	
		(ii)	<ul style="list-style-type: none"> Separate <u>memory for data and instructions</u> / Multiple memory units Different (sets of) buses one for <u>instructions</u> & one for <u>data/ instructions and data</u> can be accessed concurrently. 	1	
	(b)		<ul style="list-style-type: none"> Higher/faster clock speed More cores//dual/quad/etc core More cache memory. 	2	<p>Answers must refer to an improvement (more/higher/faster) not just "change the clock speed" Allow discussions of level 1/level 2 cache sizes for one mark.</p> <p>Accept valid features of CPUs that would improve performance e.g. Use of: Pipelining Simultaneous Multithreading</p> <p>Do not accept RISC/CISC.</p>
		(iii)	<ul style="list-style-type: none"> One instruction can be fetched while another is being decoded... ...and another is executed The output of one <u>process/instruction</u> is the input of the next. Concurrent processing of multiple instructions // completing multiple FDE cycles at once 	3	<p>For BP1, allow any 2 of the 3 parts of the FDE cycle For BP2, must give the other part of the FDE cycle not given in BP1</p> <p>Do not award if explaining multiple cores working on different parts of FDE cycle</p>
		(iv)	<ul style="list-style-type: none"> More <u>instructions</u> can be carried out in a set amount of time // less time to execute the same number of <u>instructions</u> Increasing the speed/performance/efficiency of the computer/program // quicker for the program to complete 	2	<p>Do not allow "each instruction is quicker to execute".</p> <p>BP2 has to be specific to the charity e.g. processing more donations</p>
	(d)	(i)	<ul style="list-style-type: none"> Holds all input/output Holds results of calculations (from the ALU) Checked for conditional branching (e.g. BRZ) Stores data which has come from the MDR/RAM 	2	
		(ii)	<ul style="list-style-type: none"> Holds the <u>address/location</u> of the next instruction (to be executed/fetched) Contents copied to the MAR at start of FDE Incremented (by one) on every cycle Can be changed by branch/jump instructions 	2	
		(iii)	<ul style="list-style-type: none"> Memory Address Register // MAR Memory Data Register // MDR Current Instruction Register // CIR Index Register // IR 	3	Allow Memory Buffer Register for MDR

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1	(d)	(i)	<p>1 mark per bullet up to a maximum of 2 marks, e.g:</p> <ul style="list-style-type: none"> Uses separate memory blocks for instructions and data Has separate buses (data and address) for data and instructions Has fixed memory sizes for data and Instructions Instruction memory may be ROM 	<p>2</p> <p>AO1.1 (1)</p> <p>AO1.2 (1)</p>	Accept unit instead of blocks (BP1)
1	(d)	(ii)	<p>1 mark per bullet up to a maximum of 2 marks, e.g:</p> <ul style="list-style-type: none"> Fixed instruction size No need for memory to be shared between data and instructions Removes need for secondary storage Instructions would never be changed 	<p>2</p> <p>AO2.1 (2)</p> <p>Any 2 (Max 2)</p>	

1	(a)	i	<ul style="list-style-type: none"> • Clock speed • Number of cores • Cache 	2 AO1.1	Accept Use of pipelining/size of pipeline Use of out of order execution Use of SIMD instructions Integrated graphics processing on CPU
	(b)		<ul style="list-style-type: none"> • Concurrent processing of multiple instructions • One instruction can be fetched while previous is being decoded... • And the one before is being executed. • In case of a branch pipeline is flushed. • Increases speed of execution 	3 AO1.1	
6	(a)	i	<ul style="list-style-type: none"> • Temporary storage/memory location... • ...inside the CPU • Used for a single specific purpose • Faster access speed than RAM / secondary storage 	2 AO1.1	

1	(a)		1 mark per bullet up to a maximum of 2 marks, e.g. <ul style="list-style-type: none"> • Uses the same memory for data and instructions • Uses the same bus for data and instructions • Can only fetch either data or instructions at one time/follows FDE 	2 AO1.1 (1) AO2.1 (1)	Allow: <ul style="list-style-type: none"> • ALU for arithmetic Logic Unit • CPU contains an Arithmetic Logic Unit • CPU contains a single Control Unit. Same (Memory) location is not acceptable for BP1
1	(b)	(i)	1 mark per bullet up to a maximum of 4 marks, e.g.: <ul style="list-style-type: none"> • Data/address is copied from PC to MAR • PC is incremented (by 1) (this can be in any location from here down) • Data in MAR is passed onto the Address Bus • Read signal is sent onto the control bus • RAM copies the data from the location specified by the address bus onto the data bus • Data on the data bus is passed into the MDR • Data is copied from the MDR to the CIR 	4 AO1.1 (2) AO2.1 (2)	The bullets must be in the correct order, except BP2, which can come anywhere from BP2 onwards

d	<ul style="list-style-type: none"> more than one processing unit in a (single) processor ...which can independently process instructions at the same time. 	2	AO1.1
c	<ul style="list-style-type: none"> The value <u>16</u> is copied to the MAR The contents of the of the ACC (i.e. 9) are copied to the MDR The value <u>9</u> is copied to location <u>16/count</u> 	2	AO2.2

1 per -, max 2

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3	<p>Mark Band 3—High Level (7-9 marks) The candidate demonstrates a thorough knowledge and understanding of factors affecting processor performance; the material is generally accurate and detailed. The candidate is able to apply their knowledge and understanding directly and consistently to the context provided. Evidence/examples will be explicitly relevant to the explanation. The candidate provides a thorough discussion which is well-balanced. Evaluative comments are consistently relevant and well-considered. There is a well-developed line of reasoning which is clear and logically structured. The information presented is relevant and substantiated. Candidate has used appropriate technical terminology throughout. There are few if any spelling errors or errors of grammar.</p> <p>Mark Band 2 –Mid Level (4-6 marks) The candidate demonstrates reasonable knowledge and understanding of factors affecting processor performance; the material is generally accurate but at times underdeveloped. The candidate is able to apply their knowledge and understanding directly to the context provided although one or two opportunities are missed. Evidence/examples are for the most part implicitly relevant to the explanation The candidate provides a reasonable discussion, the majority of which is focused. Evaluative comments are for the most part appropriate, although one or two opportunities for development are missed. There is a line of reasoning presented with some structure. The information presented is in the most part relevant and supported</p>	9	<p>Number of cores has an impact... Each core is a processing unit... Giving the potential for multiple instructions to be run simultaneously. Depending on the situation 4 cores running at 100MHz may perform better than 1 core running at 300MHz.</p> <p>The amount of cache (and levels) will benefit performance... Cache helps reduce the bottleneck caused by RAM being slow. No matter how fast the clock speed, the access time to RAM will always be a limiting factor.</p> <p>Contemporary processors have performance enhancing features such as pipelining and out of order execution. Harvard architecture processors benefit from having separate data and instruction memories.</p> <p>In conclusion one cannot judge performance solely on clock speed as... A processor without cache may be outperformed by a processor with a slower clock speed but access to cache. Processors will have other performance enhancements such as pipelining.</p> <p><i>Points above are for example only. Not all are needed for full marks nor do they represent all possible correct</i></p>
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1	a	i	<ul style="list-style-type: none"> - (Single) Control Unit - (Single) Arithmetic Logic Unit - (Special) registers within CPU - Instructions and Data stored in same area of memory - Instructions and Data stored in same format - A single set of buses / same bus for instructions & data (to connect CPU to Memory and I/O) <p>(1 Mark per -, Max 2)</p>	2 (AO1.1)	Accept acronyms ALU,CU
		ii	<p>Two separate areas of memory... ...one for instructions & one for data./instructions and data can be accessed concurrently.</p> <p>Different (sets of) buses... ... one for instructions & one for data./ instructions and data can be accessed concurrently.</p> <p>Pipelining... ...whilst an instruction is being executed the next can be decoded and the subsequent one fetched.</p> <p>Use of Cache... ...A small amount of high performance memory is (next to the CPU) / which stores frequently used data/instructions</p> <p>Virtual cores/Hyper-threadingTMTreating a physical core as two virtual cores.</p> <p>Multiple Cores... ...Each core acts as a separate processing unit.</p> <p>Onboard Graphics... ...Built in circuitry for graphics processing.</p> <p>(1 Mark for identifying feature, 1 mark for description)</p>	2 (AO1.2)	<p>Accept any reasonable description.</p> <p>Do not accept "64-bit"</p> <p>e.g. Performance boosting mode... ...Clock speed can be temporarily increased for performance boost.</p> <p>Out of Order Execution... ...Instructions can be executed before earlier ones if they are ready.</p> <p>Super Scalar... ...Multiple instructions can be executed simultaneously</p>
		ii	<ul style="list-style-type: none"> - The value 11 is stored in the MAR. - 11 is sent down the address bus. - A read signal is sent down the control bus. - 0 is sent (back from memory) down the data bus. - 0 is stored in the MDR... - ...and then copied to the ACC <p>(1 Mark per -, max 6)</p>	6 (AO1.2)	

1	a	i	-Small piece of memory/used for storing data (1) -Within the processor (1)	2 AO1.1	Accept 'location' for MP1
		ii	-Single control unit (1) -Single ALU (1) -Follows fetch, decode, execute cycle (1) -Data and Instructions stored in the same memory / format(1) (Max 1)	1 AO1.1	Do not accept use registers – in the question
	b		-STA	1 AO1.2	Accept STO
	c	i	-The location of the next instruction (to be fetched).	1 AO1.2	Do not accept 'Line number'
		ii	- BRZ - BRP - BRA (1 per -, max 2)	2 AO1.2	Accept 'Branch if Zero' or 'Branch if Positive' or 'Branch Always'
2			<p>Mark Band 3–High Level (7-9 marks) The candidate demonstrates a thorough knowledge and understanding of a wide range of ways a computer's performance can be improved and justifies how these measures improve performance; the material is generally accurate and detailed. The candidate is able to apply their knowledge and understanding directly and consistently to the context provided. Evidence/examples will be explicitly relevant to the explanation. The candidate provides a thorough discussion which is well-balanced. Evaluative comments are consistently relevant and well-considered. <i>There is a well-developed line of reasoning which is clear and logically structured. The information presented is relevant and substantiated.</i></p> <p>Mark Band 2 –Mid Level (4-6 marks) The candidate demonstrates reasonable knowledge and understanding of a range of methods of improving a computer's performance and justifies how many of these improve performance; the material is generally accurate but at times underdeveloped. The candidate is able to apply their knowledge and understanding directly to the context provided although one or two opportunities are missed. Evidence/examples are for the most part implicitly relevant to the explanation. The candidate provides a reasonable discussion, the majority of which is focused. Evaluative comments are for the most part appropriate, although one or two opportunities for development are missed. <i>There is a line of reasoning presented with some structure. The information presented is in the most part relevant and supported by some evidence.</i></p> <p>Mark Band 1-Low Level (1-3 marks) The candidate demonstrates a basic knowledge of how a computer's performance can be improved. Limited understanding is shown of how these measures improve performance; the material is basic and contains some inaccuracies. The candidate</p>	9 AO1: Knowledge and Understanding AO1.1 (2) AO1.2 (2) AO2.1 (2) AO3.3 (3)	<p>The following is indicative of possible factors/evidence that candidates may refer to but is not prescriptive or exhaustive:</p> <p>Methods of improving performance</p> <ul style="list-style-type: none"> - Replace CPU with faster CPU - Add more/Faster RAM - Add a graphics card - Upgrade to faster secondary storage - Update OS - Install a lighter weight OS - Defragment the hard disk - Check for viruses and spyware. <p>AO2.1: Application</p> <p>The selected knowledge/examples should be directly related to the specific question. The example below is not prescriptive or exhaustive:</p> <ul style="list-style-type: none"> - A newer CPU may have a faster clock speed and so execute more instructions per second. It may have multiple cores and so be able to execute several programs simultaneously (or one in parallel). It may have more cache meaning comparatively slower RAM can be accessed less frequently. - More RAM means more programs can be open simultaneously

	<p>makes a limited attempt to apply acquired knowledge and understanding to the context provided. The candidate provides a limited discussion which is narrow in focus. Judgments <u>if made</u> are weak and unsubstantiated. <i>The information is basic and communicated in an unstructured way. The information is supported by limited evidence and the relationship to the evidence may not be clear.</i></p> <p>0 marks No attempt to answer the question or response is not worthy of credit.</p>	<p>without the need to use much slower virtual memory.</p> <ul style="list-style-type: none"> - Adding a graphics card will speed up the rendering of 3D graphics as GPU has specialist instructions and can apply the same instruction to multiple pieces of data simultaneously. - The slower the secondary storage the longer it takes to load files/program/data. A faster secondary storage device can improve this. May choose to use flash memory (i.e. SSD) - OS makers often release updates and some of these will improve performance. - Some lighter weight operating systems use fewer system resources allowing the system to devote more to running the user's applications. - A fragmented HDD runs slowly as time is spent finding parts of the files. This is reduced by defragmenting and storing the parts of the file contiguously. - Malware can slow down a computer. Removing it will improve performance. <p>AO3.3: Evaluation</p> <p>The following is indicative of possible evaluation points that candidates may refer to but is not prescriptive or exhaustive:</p> <p>Hardware improvements (i.e. CPU, RAM, secondary storage and GPU) have costs attached but likely to have most impact.</p> <p>The higher performance the hardware, the more cost incurred.</p> <p>(NB candidates aren't expected to know relative costs of components.)</p> <p>GPU unlikely to benefit student in this scenario (unless their course requires</p>
		<p>graphics processing).</p> <p>Defragmenting HDD is free and so should be performed.</p> <p>Running anti-malware programs is free/low cost and should be done as a precaution against losing data anyway.</p> <p>Moving to lighter weight software can potentially be free if the user considers open source software.</p>

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b	i	<ul style="list-style-type: none"> • Gives more cycles per second • More instructions can be executed per second • So the program takes less time to run (1 per -, Max 2) 	<p>2</p> <p>AO1.2</p>	<p>Do not accept '...data is processed quickly...' as BP3</p>
	ii	<ul style="list-style-type: none"> • More space for data/instructions in cache memory • RAM needs to be accessed less frequently • Accessing cache is quicker than accessing the RAM (1 per -, Max 2) 	<p>2</p> <p>AO1.2</p>	

1	a	<ul style="list-style-type: none"> - An instruction can be fetched as the previous one is being decoded ... - ... and the one before that is being executed. - E.g. LDA Zero can be fetched, while OUT is being decoded and start LDA one is being executed. (1 per -)	3	
	b	<ul style="list-style-type: none"> - BRP could be followed by one of two possible instructions, which one will only be determined at execution - Meaning the wrong one may be fetched / decoded (1 per -)	2	
	c	<ul style="list-style-type: none"> - Clock speed - Cache Size - Number of cores (1 per max 1) 	1	
Total			6	
2		Pipelining would allow one instruction to be fetched as the previous one is being decoded and the one before that is being executed.(1) For example OUT could be fetched (1). As there are no jump/branch instructions it pipelines well (as there is no need to flush the pipeline). (1)	3	Accept any valid example from the given code.
1		<ul style="list-style-type: none"> • Control bus... • ...transmits control signals from the control unit (to other parts of the processor) • Data bus... • ...carries the data (from one place to another) • Address bus... • ...carries the location address (register) where the data is going (to or from) 	6	These are the expected responses as they are the buses listed in the specification, however, other responses are acceptable, for example named buses like 'EIDE, a local bus' and 'Video bus to maintain screen display'. Serial and parallel buses are not acceptable because they are not named. Not a memory bus. Control bus does not send program instructions. Examples would include interrupt signals / read / write operation carried out Examiner's Comments Understanding of the purpose of the three bus types named in the specification continues to improve although there is still the desire among candidates to imbue them with rather more power than they have got. Typical is the desire to say that the bus 'stores' something rather than acting as a conduit. On a base level candidates can picture data being sent around the processor in the data bus and the details of where it is being sent to are carried in the address bus. The control bus simply passes the control signals to the registers from the control unit.

3		<ul style="list-style-type: none"> • Temporary storage • for data being processed / during calculations • I/O in processor... • ... used as a buffer / gateway 	4	<p>Examiner's Comments</p> <p>A good discriminator question, with candidates achieving a range of marks.</p>
4		<p>Mark band 6-8. High level response. Candidate has given a comprehensive response stating most of the bullets for all three points and has used appropriate technical language throughout their answer. There are few, if any, spelling or grammatical errors.</p> <p>Mark band 3-5. Medium level response. Candidate has given an adequate response stating some of the bullets for all three points or has explained two comprehensively. The candidate has used some appropriate technical language in their answer. There may be a few spelling or grammatical errors.</p> <p>Mark band 0-2. Low level response. Candidate has given an adequate response stating some of the bullets for two points or has explained one comprehensively. The candidate may have used some appropriate technical language in their answer. There are some spelling or grammatical errors.</p> <ul style="list-style-type: none"> • Registers <ul style="list-style-type: none"> ◦ Mentions CIR MDR MAR PC and ACC ◦ Jump instruction CIR sends address to PC ◦ PC incremented ◦ MDR copies data to CIR ◦ CIR holds the data to be decoded.. ◦ ...into opcode and operand • Saving <ul style="list-style-type: none"> ◦ CIR sends address to MAR.. ◦ ...sends data to MDR ◦ All data to be saved uses the ACC • Other relevant points <ul style="list-style-type: none"> ◦ All arithmetic and logical operations use the ACC ◦ Mention of buses (Address Data or Control) ◦ Control unit for synchronisation ◦ Mention of Interrupt Register ◦ ALU performs calculations 	8	<p>accept: Memory Buffer Register</p> <p>Examiner's Comments</p> <p>As was expected for the banded response question all candidates could write something about the registers and almost all of those could write something about a jump instruction. There were some good write-ups about the use of the accumulator and the ALU, some mentioned the use of buses, but Control Unit and Interrupt register were a rare find. Saving was a bit patchy with some rather vague descriptions although there were still the occasional gems to be found. A good spread of responses overall.</p>

**If you found this
useful, drop a follow
to help me out!**

THANK YOU!

GCST