GCST

1.1.2
TYPES OF PROCESSOR

TOPIC WISE EXAM QUESTIONS

ANSWERS

A-LEVEL OCR

1	(b)		• CISC has a larger instruction set • RISC has a smaller instruction set • CISC is difficult to pipeline • RISC is easier to pipeline • CISC tends to have more addressing modes • RISC tends to have fewer addressing modes • CISC **instructions** may take multiple clock cycles to execute • RISC **instructions** take one clock cycle to execute	AO1.2 (2)	Accept any other valid points Mark in pairs
			• CISC has complex circuitry/more transistors. • RISC has less complex/simple circuitry • CISC uses less RAM • RISC uses more RAM		
1	(c)		• Parallel processing will allow multiple separate jobs/instructions/FDE cycles to run concurrently. • Longer rendering jobs can be split, shortening the overall time taken. • Different CPUs/cores can tackle different frames/sections/components of the video simultaneously.	AO1.2 (1) AO2.1 (2)	

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2022

	(e)		**Mark Band 3–High Level (9-12 marks)** The candidate demonstrates a thorough knowledge and understanding of both CISC and RISC. The material is generally accurate and detailed. The candidate is able to apply their knowledge and understanding directly and consistently to the context provided. Evidence/examples will be explicitly relevant to the explanation. The candidate provides a thorough discussion which is well balanced. Evaluative comments are consistently relevant and well-considered. There is a well-developed line of reasoning which is clear and logically structured. The information presented is relevant and substantiated. **Mark Band 2-Mid Level (5-8 marks)** The candidate demonstrates reasonable knowledge and understanding of CISC and/or RISC; the material is generally accurate but at times underdeveloped. The candidate is able to apply their knowledge and understanding directly to the context provided although one or two opportunities are missed. Evidence/examples are for the most part implicitly relevant to the explanation. The candidate provides a sound discussion, the majority of which is focused. Evaluative comments are for the most part appropriate, although one or two opportunities for development are missed. There is a line of reasoning presented with some structure. The information presented is in the most part relevant and supported by some evidence. **Mark Band 1-Low Level (1-4 marks)** The candidate demonstrates a basic knowledge of CISC or RISC; the material is basic and contains some inaccuracies. The candidate makes a limited attempt to	12 AO1.1 (2), AO1.2 (2), AO2.1 (3), AO3.3. (5)	AO1 CISC is a complex instruction set. The traditional approach to processor design. Lots of instructions available although some instructions in CISC will rarely get used. RISC is a reduced instruction set. A smaller number of instructions available, several instructions can be combined to perform the same tasks as CISC processors. RISC instructions are used regularly. RISC has fewer transistors/less complex circuitry whereas CISC integrated circuits are more expensive/complicated. RISC instructions take one cycle whereas CISC may take several. RISC can only do complex things by combining multiple instructions whereas CISC is done in one line. Compilers for RISC need to be more complex than compilers for CISC AO2 CISC processors would run the same software as the desktop machines. Would be less power efficient and require larger battery and cooling mechanisms. More expensive to purchase. RISC processor requires software to be written specifically for it (cannot use CISC instructions). More power efficient and so requires less/no cooling and smaller battery/longer battery life. RISC devices may require greater RAM as programs tend to be larger than their CISC equivalents. AO3 Mobile use of CISC would save money on software and increase compatibility but cost more to purchase and be physically larger (heat sink/larger battery) and/or have a shorter battery life. RISC would require investment in software but be cheaper to purchase and give a better performance out of the office (lighter/longer battery life). Some compatibility issues may be reduced with emulators and translators.

2021

	iii	• Performing complex numerical calculations • Calculations on matrices / vectors / multiple data at the same time • …e.g. insurance pricing, modelling risk, calculating bills	2 AO2.2	Example has to relate to insurance company

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2020

AS - Level

6	(c)		1 mark per bullet up to a maximum of 2 marks, e.g: • Some instructions in CISC will rarely get used … • … In RISC instructions are used regularly • In assembly for CISC, a statement that takes one mnemonic … • … (may) take multiple mnemonics in RISC • Compilers for RISC need to be more complex … • … than compilers for CISC • CISC architecture has complex circuitry and is therefore more expensive to manufacture... • ...RISC architecture has simple circuitry minimising manufacture cost.	2 AO1.1 (1) AO1.2 (1)	Accept More than one clock cycle for each instruction in CISC ... ...one clock cycle for each instruction in RISC For BP's 3 and 4

2018

		iii	- RISC has a smaller instruction set (than CISC) - Requires fewer transistors / less complex circuitry - Means less power is required. (1 Mark per -, Max 3)	3 (AO1.2)	

AS - Level

	c		*advantage* - Costs less to design/produce. *because* - Requires less cooling to be built in. - (If battery powered) can run off smaller battery. - Has fewer instructions than other (CISC) processors. - Simpler (circuit/hardware) design/manufacture. - Fewer transistors. *(1 per -, max 2, 1 max from 'because' group)*	**2** **AO2.1** **(2)**	

2017

1	a	i	To render models of proposed buildings. (1) Run CAD software. (1) Run modelling calculations. (1) Any example sensible to scenario. (1) (Max 1)	1 (AO2.1)	

2			• CPUs are general purpose processors (1) whereas GPUs are designed specifically for graphics (1). And so likely to have built in circuitry / instructions for common graphics operations (1). GPUs are able to perform an instruction on multiple pieces of data at one time (1) often we want to do this when processing graphics (e.g. transforming points in a polygon or shading pixels) (1) which means it can perform transformations to onscreen graphics quicker than a CPU (1).	3	Up to 3 marks for a valid explanation.

				3	Processors have increasingly large clock speeds and can be overclocked.
3			The candidate is able to apply their knowledge and understanding directly and consistently to the context provided. Evidence/examples will be explicitly relevant to the explanation. The candidate is able to weigh up both sides of the argument which results in a supported and realistic judgment as to which approaches to provide increasingly larger amounts of computing power are best. *There is a well–developed line of reasoning which is clear and logically structured. The information presented is relevant and substantiated.* **Mark Band 2–Mid Level (5–8 marks)** The candidate demonstrates reasonable knowledge and understanding of methods of utilising large amounts of computing power; the material is generally accurate but at times underdeveloped. The candidate is able to apply their knowledge and understanding directly to the context provided although one or two opportunities are missed. Evidence/examples are for the most part implicitly relevant to the explanation. The candidate makes a reasonable attempt to come to a conclusion showing some recognition of which approaches to provide increasingly larger amounts of computing power are best. *There is a line of reasoning presented with some structure. The information presented*	5	Processors can have multiple cores. Super computers can have multiple processors (and GPUs). GPUs can be applied to problems other than graphics processing. Problems can be distributed across a number of computers working together. **AO2.1: Application** Having multiple cores can speed up smaller problems but this will not be enough for larger problems. Supercomputers are prohibitively exceptionally expensive to buy and run for all but large organisations. GPUs are becoming a cost efficient way of tackling problems. GPUs tend to have large number of cores so can run on highly paralleliseable problems... …but only where the same instruction is being applied to multiple pieces of data (SIMD) **AO3.3: Evaluation** Increased clock speed is limited to smaller problems. Even doubling the clock speed would only halve the time taken. Parallel processing isn't suited to all problems. Most problems are only partially parallelisable. Writing algorithms for parallel processing is more challenging than GPUs suited to a subset of science/ engineering problems where the same calculation is repeated on multiple data sets.

1	a	i	*CISC:* Each instruction may take multiple cycles Single register set Instructions have variable format Many instructions are available Many addressing modes are available Complicated processor design Integrated circuit is expensive *RISC:* An instruction performs a simple task Limited number of instructions available Complex tasks can only be performed by combining multiple instructions Simple processor design	4	Max 3 marks for either CISC or RISC, total max 4 **Examiner's Comments** There were a wide variety of answers to this question, ranging from the very accurate to the very vague. A significant number of candidates said that RISC is used in mobile phones, if the question had asked for an example this would probably have been a good one. Those that missed marks here generally talked about the programming and its relative difficulty on either type of processor rather than the processor itself.
		ii	Programs run faster… …due to simpler instructions	2	**Examiner's Comments** Most candidates got the first mark, the more able candidates managed to get the second, again, here the most common erroneous answer was about the merits/drawbacks of programming.
	b	i	Calculations are done by the maths co-processor… …so processing is faster …when using floating point arithmetic	2	**Examiner's Comments** Both this and the next question were well answered by candidates who knew that a co-processor is for floating point calculations.
		ii	No increase in speed… …as co-processor not suitable for task / as there are no calculations	2	**Examiner's Comments** For this part there was a wide variety of inventions as to how a co-processor could control a print queue, not answered well by those who did not grasp the first part of the question.

2		i	• Single control unit • One instruction at a time • Uses fetch execute **cycle** • Program & data stored together / program & data in same format	3	Accept single ALU Allow FDE Location TV **Examiner's Comments** A significant amount of candidates gave a single processor as a response to this question which was judged to not be sufficient for this level of examination.
			Total	3	
3	a		• CISC is more complex / RISC is simpler / CISC longer instruction set • RISC requires more RAM • CISC many address modes • CISC may have more registers • RISC takes one machine cycle / CISC takes many cycles to complete one instruction • RISC fixed number of bytes / CISC variable number	4	**Do not accept "task" in place of "instruction".** **Examiner's Comments** A fair number of responses were still mentioning cost as a difference: the Principal Examiner felt this response was not contextualised to computing and as such no credit was allowed for this.
	b		• Fetch- The next instruction is fetched from main memory/address • Decode- The instruction is interpreted / translated / split into opcode and operand (in the CIR) • Execute- The appropriate instruction/opcode is carried out on the operand.	3	**Fetch they may describe the whole cycle** **Not translated in MDR** **Examiner's Comments** A lot of candidates are unsure as to what actually happens in the fetch decode execute cycle and some very vague answers were provided. However, there were a few excellent responses that did show a good understanding of the processes.

If you found this useful, drop a follow to help me out!

THANK YOU!

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