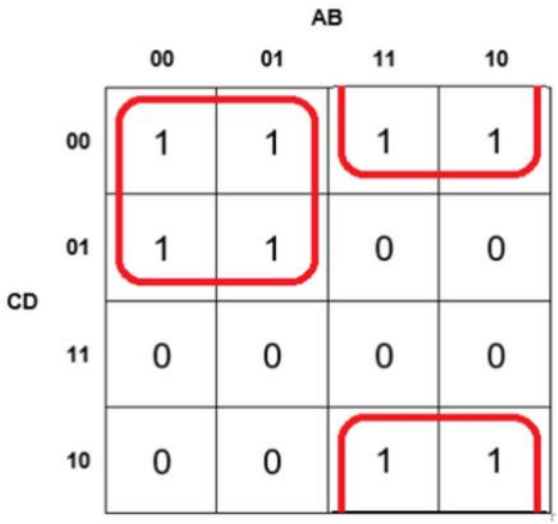
GCST

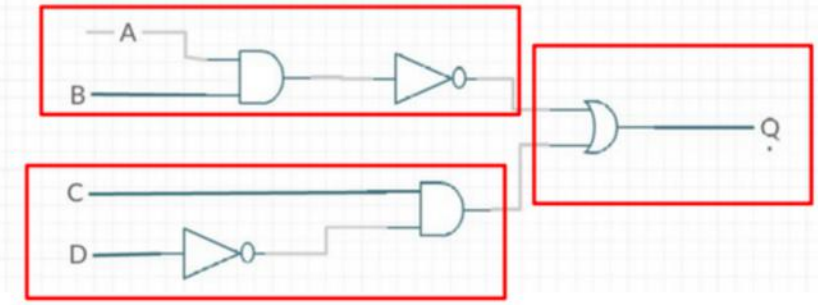
1.4.3
BOOLEAN ALGEBRA
TOPIC WISE EXAM QUESTIONS
ANSWERS

A-LEVEL OCR

6	(a)	(i)	• ¬ (A ˅ B) // NOT (A OR B) • ⊻ C // XOR C	2	First MP requires brackets, NOT A or B is incorrect. Can be written in different order (e.g. C XOR NOT (B OR A) as long as logically correct. Accept $\overline{(A + B)} \oplus C$
6	(a)	(ii)	• 1 mark for first two rows (1,0) • 1 mark for next two rows (0,1) • 1 mark for next four rows (0,1,0,1)	3	

A	B	C	P	Marking Guidance
0	0	0	**1**	1 Mark
0	0	1	**0**	
0	1	0	**0**	1 Mark
0	1	1	**1**	
1	0	0	**0**	1 Mark
1	0	1	**1**	
1	1	0	**0**	
1	1	1	**1**	

6	(b)		• Correct highlighting on K map as shown • $\overline{A}.\overline{C}$ // NOT A AND NOT C... • A ∧ $\overline{D}$ // A AND NOT D... • ...v // + // OR joining the 2 correct expressions together	4	 Do not penalise candidates who attempt to simplify even further (e.g. NOT A AND NOT C = NOT (A OR C) using De Morgan's). MP1 - correct answer only MP4 is dependent on MP2 & 3

5	(a)	Solution: 1 mark per bullet up to a maximum of 4 marks: • 1 mark for filling in the table correctly • 1 mark for the group shown in red • 1 mark for the group shown in green • 1 mark for the simplified expression $A \vee (C \wedge D)$	4 AO2.1 (2) AO2.2 (2)	Brackets are not required for the simplified expression
5	(b)	 1 mark per bullet up to a maximum of 3 marks: • An AND gate taking A and B as inputs with the output connecting to a NOT gate • An AND gate taking C and the NOT of D as the inputs • An OR gate taking the outputs of the NOT and AND gates	3 AO3.1 (3)	Allow NAND gate as alternative for BP1

	AB	AB	AB	AB
	00	01	11	10
CD 00	0	0	1	1
CD 01	0	0	1	1
CD 11	1	1	1	1
CD 10	0	0	1	1

<table>
<tr><td>5</td><td>(a)</td><td></td><td>Q ≡ A ∧ B
∧
(C ∨ D)</td><td>3

AO1.2</td><td>Q ≡ A ∧ B ∧ (C ∨ D)

Accept alternative symbols for AND / OR
e.g. Q = A AND B AND (C OR D)
Brackets must be included for 3rd point
Allow XOR for bullet point 3
Any additional symbols max 2 marks</td></tr>
<tr><td></td><td>(b)</td><td>i</td><td>• Identification of De Morgan's and/or double negation rule
• Correct final answer to give A v B</td><td>2

AO2.2</td><td></td></tr>
<tr><td></td><td>(c)</td><td>i</td><td>S = A ⊻ B
C = A ∧ B</td><td>2

AO2.1</td><td>Accept alternative symbols for AND /XOR</td></tr>
<tr><td></td><td></td><td>ii</td><td>• 1 mark for S column
• 1 mark for C column</td><td>2

AO2.1</td><td><table><tr><th>A</th><th>B</th><th>S</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr></table></td></tr>
<tr><td></td><td></td><td>iii</td><td>• Logic circuit adds together 2 binary digits / half adder</td><td>4</td><td></td></tr>
<tr><td></td><td></td><td></td><td>• S gives sum, C gives carry
• Two half adders can be joined together…
• …with an OR gate
• to form full adder
• 4 full adders can be used to add two four bit numbers
• Carry out on one joined to carry in on next</td><td>AO1.2</td><td></td></tr>
</table>

GCST

2020

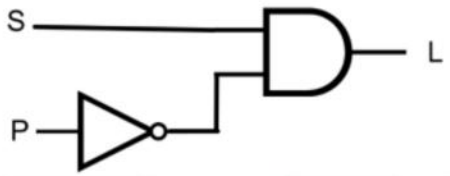
4	(a)	i	• left column filled with 1s (¬ A ∧ ¬ B) … • right column filled with 1s (A ∧ ¬ B)… • …Middle 2 columns filled with zero or blank	3 AO1.2 (1) AO2.2 (2)	AB CD 00 01 11 10 00 1 0 0 1 01 1 0 0 1 11 1 0 0 1 10 1 0 0 1
4		ii	• ¬ B / NOT B • Karnaugh map used to show 1s highlighted with overlap	2 AO2.2	AB CD 00 01 11 10 00 1 0 0 1 01 1 0 0 1 11 1 0 0 1 10 1 0 0 1
4	(b)	i	• Delay / store a value… • …of 1 bit • When a signal is given	2 AO1.1	
4	(b)	ii	• Data input • Clock input	4	
			• Q output • When clock input goes high… • …Q changes to D • NOT Q is reverse of Q	AO1.1 (2) AO1.2 (2)	

AS - Level

7			A B C D X Marking Guidance 0 0 0 0 0 1 Mark 0 0 1 0 1 0 1 0 0 0 1 Mark 0 1 1 0 1 1 0 0 0 0 1 Mark 1 0 1 0 1 1 1 0 1 1 1 Mark 1 1 1 1 0	4 AO2.2 (4)	Award 1 mark for each group of 4 1's / 0's.

GCSE

2019

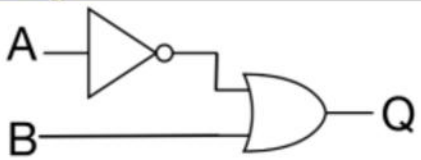
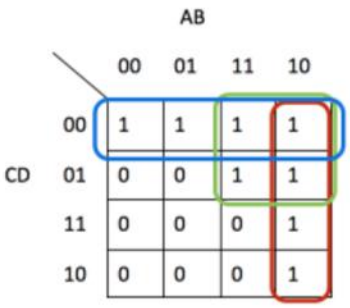
	c	i	<table><tr><th>P</th><th>S</th><th>L</th></tr><tr><td>False</td><td>False</td><td>False</td></tr><tr><td>False</td><td>True</td><td>True</td></tr><tr><td>True</td><td>False</td><td>False</td></tr><tr><td>True</td><td>True</td><td>False</td></tr></table> 1 Mark for first 2 rows, 1 Mark for second 2 rows.	2 AO1.2	Accept any sensible representation of True or False
		ii	-P going into not Gate -S going into AND gate… -…NOT P going into AND gate, L coming out of it and no additional gates or connections. (1 per -, max 3)	3 AO3.1	

AS - Level

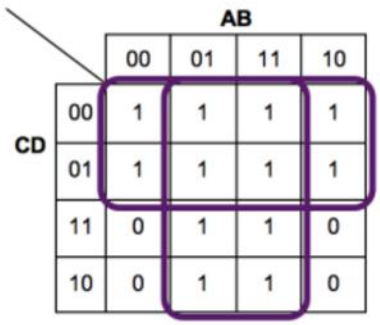
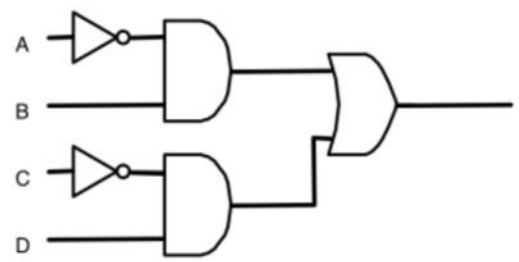
9			<table><tr><th>A</th><th>B</th><th>C</th><th>Q</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> First 4 rows correct 1 mark Last 4 rows correct 1 mark	2 (AO2.2)	

GCST

2018

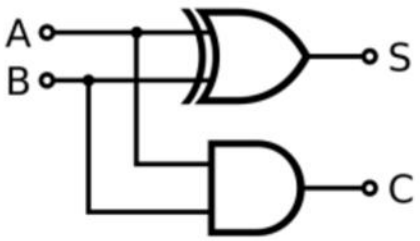
10	a		 - A going into NOT gate. - B and NOT A going into OR gate (and Q coming out of it) (1 Mark per -, Max 2)	2 (AO1.2)	
	b		-Groups correctly identified (with no further groups). - Answer includes ¬ C∧¬D - Answer includes A∧¬B - Answer includes A∧¬C - All three sections joined with ∨s in any order but with no further sections. E.g. (A∧¬B)∨(A∧¬C)∨(¬ C∧¬D) The brackets aren't necessary (1 Mark per -, Max 5)	5 (AO1.2)	

AS - Level

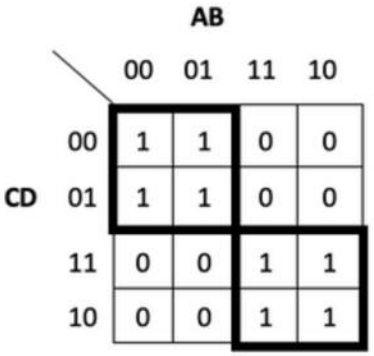
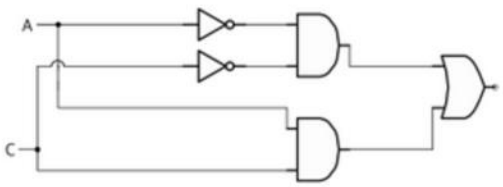
6	a		 Gives: B∨¬C - Correct two groups identified. - B∨ - ¬C (1 per -, max 3)	3 AO2.1 (1, 1st Mark) AO2.2 (2, Last 2 Marks)	Also accept: ¬C ∨ B Accept alternative symbols.
	b		- NOT gates after A and C - AND gates: one taking (NOT) A, B as inputs the other taking (NOT) C, D as inputs. - An OR gate taking in the outputs of both AND gates. - …No further gates or connections (1 per -, max 4)	4 AO2.2 (4)	

GCST

2017

4	a		Q ≡ (A∧B) ∨ (C∧D) 1 mark for (A∧B) 1 mark for (C∧D) 1 mark for the ∨ joining the two parts.	3 (AO1.2)	Accept (C∧D) ∨ (A∧B) Accept (B∧A) instead of (A∧B) Accept (D∧C) instead of (C∧D) Accept alternative notations (e.g. +/. OR/AND) Accept AB as (A.B) and CD as (C.D) Accept answers without brackets
	b	i	(see table below) 1 mark for each of the pairs of rows.	4 (AO1.2)	
		ii	(F∨G) ∧ E One mark for the (F∨G) One mark for the ∧ E	2 (AO2.2)	Accept: (G∨F) ∧ E E∧(F∨G) E∧(G∨F)
11	a		 XOR Gate (1) AND Gate (1) Correct connections and no additional gates (1)	3 (AO1,1)	

E	F	G	(E∧F)	(E∧G)	(E∧F)∨(E∧G)
1	1	1	1	1	1
1	1	0	1	0	1
1	0	1	0	1	1
1	0	0	0	0	0
0	1	1	0	0	0
0	1	0	0	0	0
0	0	1	0	0	0
0	0	0	0	0	0

11	b		- Correctly identified groups on Karnaugh map/Correct boolean statement.(1) - NOT A AND NOT C Gates (1) - A AND C gates (1) - Both sets of gates joined by OR gate (with no other gates used). (1)	4 (AO2.2)	 (¬A ∧ ¬C) ∨ (A∧C) Or equivalent.  Or equivalent.

AS - Level

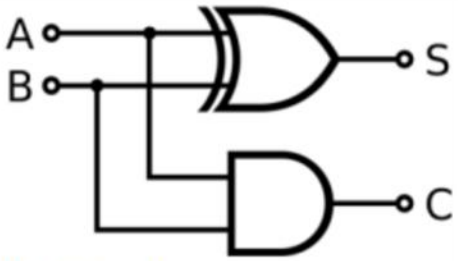
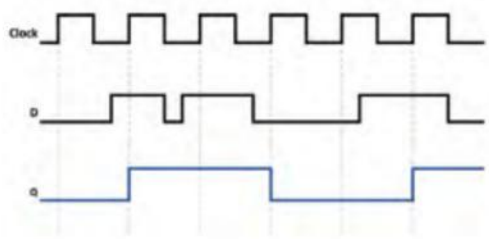
6	a			1 AO1.1	Accept diagram of gate only without input / output
	b		OR gate outputs true if at least one of its inputs is true (1) XOR gate output true if and only if one of its inputs is true. (1)	2 AO1.2	Accept appropriate, correctly labelled, truth tables. One mark for each truth table.

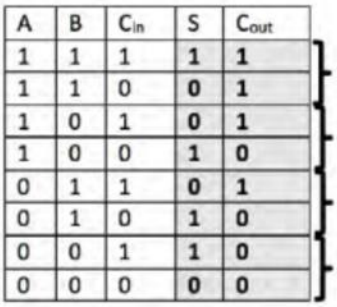
	c	i	<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Output</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> 1 Mark 1 Mark 1 Mark 1 Mark	**4** **AO2.2**	

		ii	(A ∨ B) ∨ (C ∨ D) ≡ Output A ∨ B (1 Mark) ∨ (C ∨ D) (1 Mark)	**2** **AO2.2**	Accept answer without brackets. Accept alternative notation i.e. OR , +

GCSE

EXTRA

1			 XOR Gate (1) AND Gate (1) Correct connections and no additional gates (1)	3 (AO1,1)	**Examiner's Comments** Most candidates scored well on these questions demonstrating their understanding of logic gate circuits. Some candidates simplified the circuit in part b) which achieved full marks provided the resultant circuit gave the same output.
5		i	A	1	
		ii	¬(A∨ B)	1	
		iii	A∨B	1	
4	a		To store the state of a bit	1	
	b		 One mark for each two correct clock cycles.	3	

6	a	i	 1 Mark for rows 1 and 2 1 Mark for rows 3 and 4 1 Mark for rows 5 and 6 1 Mark for rows 7 and 8	4	
		ii	– Circuit adds two bits (and a carry bit) together / is an adder. – A B and C_{in} are added together – The result is given in S – And a carry bit in C_{out} (1 per –)	4	
	b	i	$S \equiv A \veebar B \veebar C_{in}$	1	Accept XOR instead of ∨ Accept $\oplus$ instead of ∨
		ii	$C_{out} \equiv ((A \veebar B) \wedge C_{in}) \vee (A \wedge B)$ One mark for $((A \vee B) \wedge C_{in})$ One mark for $\vee (A \wedge B)$	2	Accept XOR instead of ∨ Accept $\oplus$ instead of ∨ Accept AND instead of ∧ Accept OR instead of ∨ Accept + instead of ∨

If you found this useful, drop a follow to help me out!

THANK YOU!

GCST

GCSECOMPUTERSCIENCETUTOR.COM