GCST

1.4.3
BOOLEAN ALGEBRA
TOPIC WISE EXAM QUESTIONS

A-LEVEL OCR

GCST

SPEC

1.4.3 Boolean Algebra	a) Define problems using Boolean logic. See appendix 5d. b) Manipulate Boolean expressions, including the use of Karnaugh maps to simplify Boolean expressions. c) Use the following rules to derive or simplify statements in Boolean algebra: De Morgan's Laws, distribution, association, commutation, double negation. d) Using logic gate diagrams and truth tables. See appendix 5d. e) The logic associated with D type flip flops, half and full adders.	Candidates should be familiar with AND, OR, NOT and XOR. Candidates should be familiar with the logic of each Boolean operator, and the truth tables. Candidates should be able to construct logic gate diagrams from a Boolean expression and vice-versa. Candidates should be able to construct truth tables from Boolean expressions and logic gate diagrams. Candidates should have an understanding that Boolean expressions can be simplified and should have experience of simplifying expressions using Karnaugh maps. Candidates should be able to create, complete and interpret Karnaugh maps to simplify Boolean expressions. Candidates should be aware of the given De Morgan's laws and should be able to apply these to a Boolean statement. Candidates should have experience of manipulating and simplifying Boolean statements using these rules of distribution, commutation, association and double negation. Candidates need to understand the purpose and principles of D type flip flops and how and where they are used in a computer. They should be able to recognise how they can be triggered by a clock pulse (see practice paper 2 for an example). Candidates are not expected to memorise the logic gates that make up a D-type flip flop. Candidates need to understand the purpose and function of an adder circuit, and the difference between a half and full adder. They should be able to recognise and draw the logic gates and truth tables for full and half adders.

6 (a) A computer scientist has created the following logic circuit shown in **Fig. 6**.

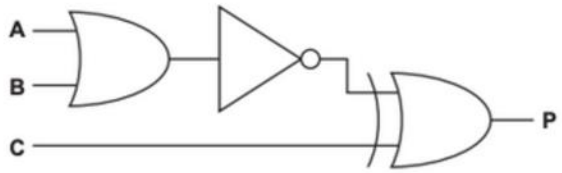

Fig. 6

(i) Give the Boolean expression that represents the logic circuit shown in **Fig. 6**. Do not attempt to simplify the expression.

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..... **[2]**

(ii) Complete the truth table for the logic circuit shown in **Fig. 6**.

A	B	C	P
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[3]

The following Karnaugh map represents another logic circuit.

CD \ AB	00	01	11	10
00	1	1	1	1
01	1	1	0	0
11	0	0	0	0
10	0	0	1	1

(b) Use this Karnaugh map to find the simplified expression for this circuit.

You should highlight the map as appropriate and write the expression here.

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..... **[4]**

5 Elliott has designed a logic circuit. The expression he has created for the logic circuit is:

$Q = (A \wedge \neg B) \vee (\neg A \wedge C \wedge D) \vee (A \wedge B)$

(a) Complete the Karnaugh Map below to simplify this expression. Show your working.

CD \ AB	00	01	11	10
00				
01				
11				
10				

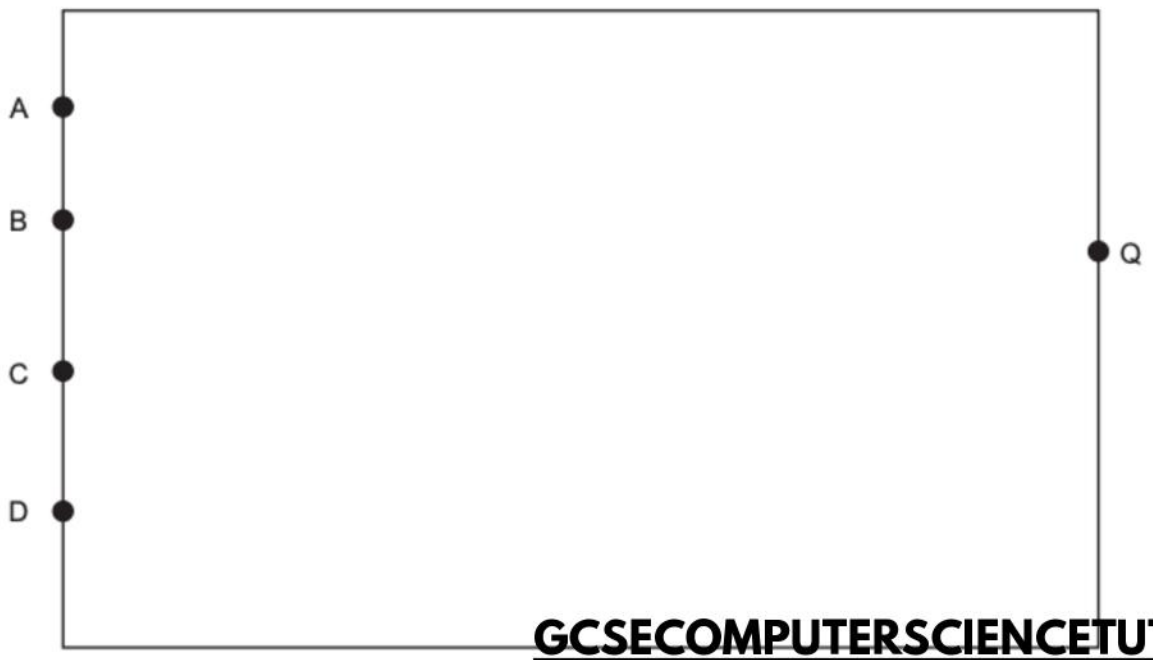
Simplified expression:

.....

..... **[4]**

(b) Draw a Logic diagram for the following expression:

$Q = \neg(A \wedge B) \vee (C \wedge \neg D)$



[3]

5 All users of a computer system have a unique username and password. The computer system has implemented two-factor authentication so that users must respond to either an email or text message containing a secret code to be able to access the system.

Let:

A be a Boolean value for if a user enters a valid username

B be a Boolean value for if a user enters a password that matches their username

C be a Boolean value for if a user is able to respond to an email containing a secret code

D be a Boolean value for if a user is able to respond to a text message containing a secret code

Q be a Boolean value for if entry to the computer system is allowed

(a) Complete the Boolean expression below:

$Q \equiv$ ..... **[3]**

(b) Another Boolean expression for a logic system is shown below:

$$Q \equiv \neg (\neg A \wedge \neg B)$$

(i) Simplify this Boolean expression so that it does not include any negation. You must explain which Boolean algebra rule(s) you are using at each step.

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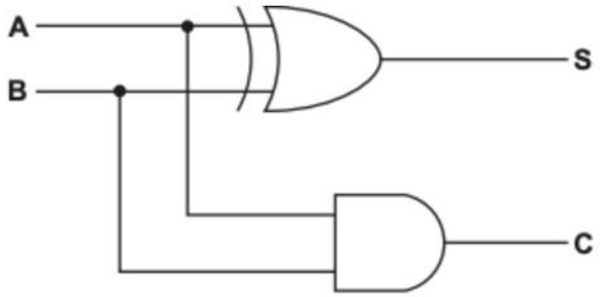

(c) The logic circuit above has two inputs (**A**, **B**) and two outputs (**S**, **C**).

(i) Give the Boolean expressions for the outputs **S** and **C**.

S ≡ .....

C ≡ .....

[2]

(ii) Complete the truth table for this logic circuit.

A	B	S	C
0	0		
0	1		
1	0		
1	1		

[2]

(iii) Describe how this logic circuit can be adapted to add together two 4-bit binary numbers.

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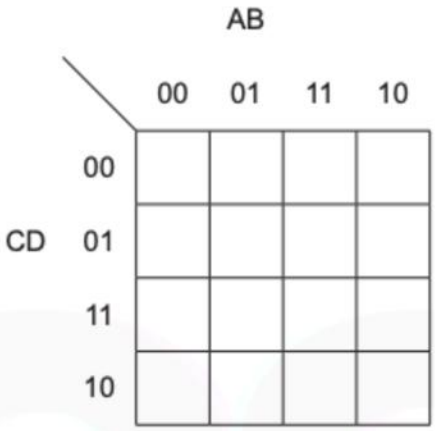
4 (a) (i) Complete the Karnaugh map below for the Boolean expression (¬ A ∧ ¬ B) ∨ (A ∧ ¬ B)



[3]

(ii) Use the Karnaugh map to find a simplified Boolean expression that is equivalent to (¬ A ∧ ¬ B) ∨ (A ∧ ¬ B)

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..... [2]

(b) (i) State the purpose of a D-type flip-flop circuit.

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(ii) Describe the inputs and outputs used by a D-type flip-flop circuit, explaining how the inputs are used to control the outputs.

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7 Daniel is an engineer. He has created the following logic circuit shown in **Fig. 4**.

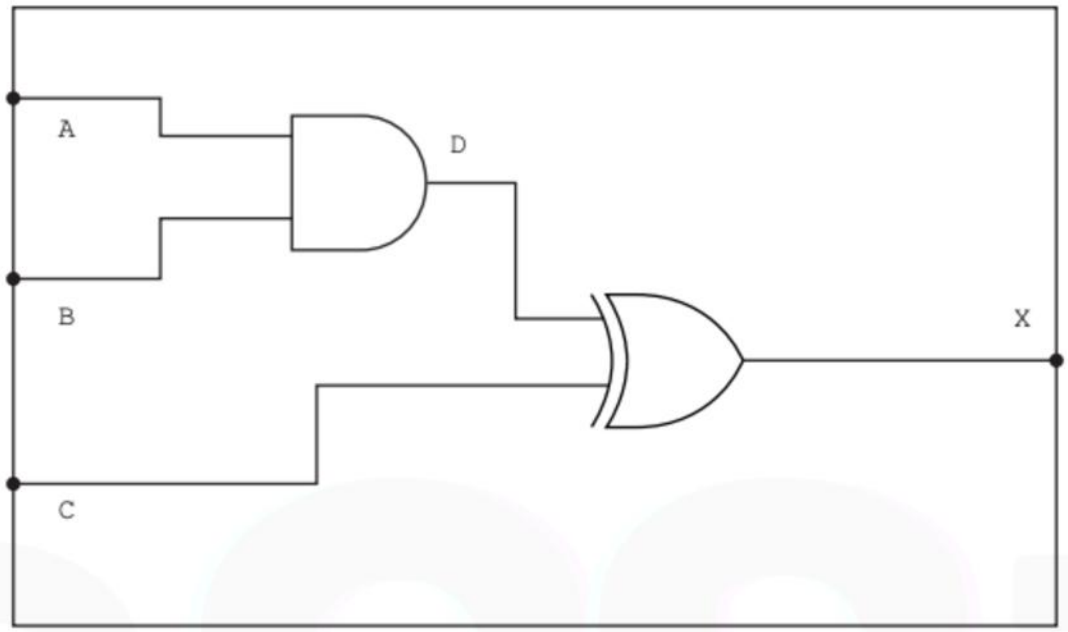

Fig. 4

Complete the truth table below for the logic circuit shown in **Fig. 4**.

A	B	C	D	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[4]

GCST

2019

1 A company releases an in-home virtual assistant called 'Bertie Butler'.

The device, when placed in a room, listens out for the phrase "Hey Bertie". When someone says that phrase it then listens to the question that follows and tries to give a relevant answer.

(c) Bertie Butler's circuitry is designed to only listen out for "Hey Bertie" under certain circumstances, which are:

The privacy button (**P**) must be off and the microphone must generate a signal (**S**) to say a sound has been heard.

(i) Complete the truth table for whether the device is listening (**L**).

P	S	L
False	False	
False	True	
True	False	
True	True	

[2]

(ii) Draw logic gates to represent the circuitry needed.

9 Complete the truth table to represent the following Boolean expression.

AS - Level

$Q \equiv \neg (A \wedge B) \vee C$

A	B	C	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[3]

GCST

2018

10 **(a)** Draw a logic gate diagram to represent the Boolean expression

$Q \equiv \neg A \vee B$

[2]

(b) Find the Boolean expression represented in the Karnaugh Map below. Show your working.

		AB			
		00	01	11	10
CD	00	1	1	1	1
	01	0	0	1	1
	11	0	0	0	1
	10	0	0	0	1

[5]

6 A Boolean expression is entered into a Karnaugh Map.

(a) Give a simplified version of the expression using the Karnaugh Map. You must show your working.

CD \ AB	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	1	1	0
10	0	1	1	0

Simplified Expression: ..... **[3]**

(b) Draw a logic gate diagram to represent the expression below. **[4]**

$(\neg A \wedge B) \vee (\neg C \wedge D)$

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2017

4 A cinema offers discounted tickets, but only under one of the following conditions:

- Customer is under 18 and has a student card.
- Customer is over 60 and has ID which proves this.

Let:

A be Customer is under 18

B be Customer has a student card

C be Customer is over 60

D be Customer has ID

Q be Discount ticket issued

(a) Complete the Boolean expression below:

$Q \equiv$ .....

[3]

(b) The cinema has a voucher which promises free popcorn when the voucher is produced whilst buying a soft drink or bottle of water.

Let:

E be Voucher is shown

F be Soft drink is bought

G be Bottle of water is bought

R be Free popcorn given.

This could be written as:

$R \equiv (E \wedge F) \vee (E \wedge G)$

(i) Complete the truth table below.

E	F	G	(E∧F)	(E∧G)	(E∧F)∨(E∧G)
1	1	1			
1	1	0			
1	0	1			
1	0	0			
0	1	1			
0	1	0			
0	0	1			
0	0	0			

[4]

(ii) Simplify the expression

$(E \wedge F) \vee (E \wedge G)$

.....

.....

[2]

11 A half adder has the truth table shown below:

A	B	Sum	Carry
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

(a) Draw a half adder using logic gates.

(b) Draw the logic gates represented by the Karnaugh Map below. Show your working.

CD \ AB	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	1	1
10	0	0	1	1

[3]

[4]

6 **(a)** Draw an XOR gate.

[1]

(b) Explain the difference in the function of OR and XOR gates.

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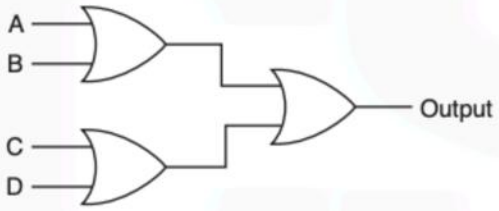
..... **[2]**

(c) A circuit contains the logic gates shown below.



(i) Complete the logic table below.

A	B	C	D	Output
1	1	1	1	
1	1	1	0	
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	
0	0	0	0	

[4]

(ii) Complete the Boolean expression below to represent the circuit.

..... ≡ Output

[2]

GCST EXTRA

1. A half adder has the truth table shown below:

A	B	Sum	Carry
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

Draw a half adder using logic gates.

[3]

5. State the simplified versions of the following Boolean expressions:

(i) ¬ ¬A

---[1]

(ii) (¬A ∧ ¬B)

---[1]

(iii) ¬(¬A ∧ ¬B)

---[1]

4(a). The component below is a D-Type, positive edge triggered, flip-flop.

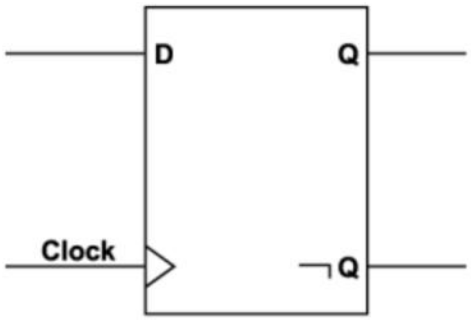


Fig. 10.2

State the purpose of a flip-flop.

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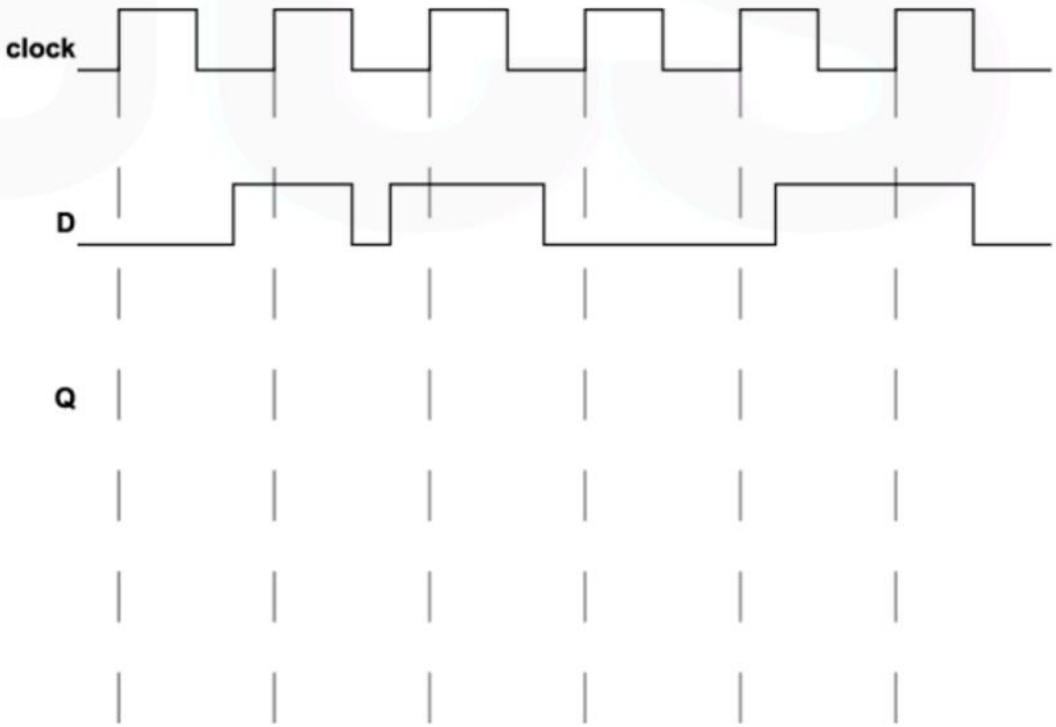
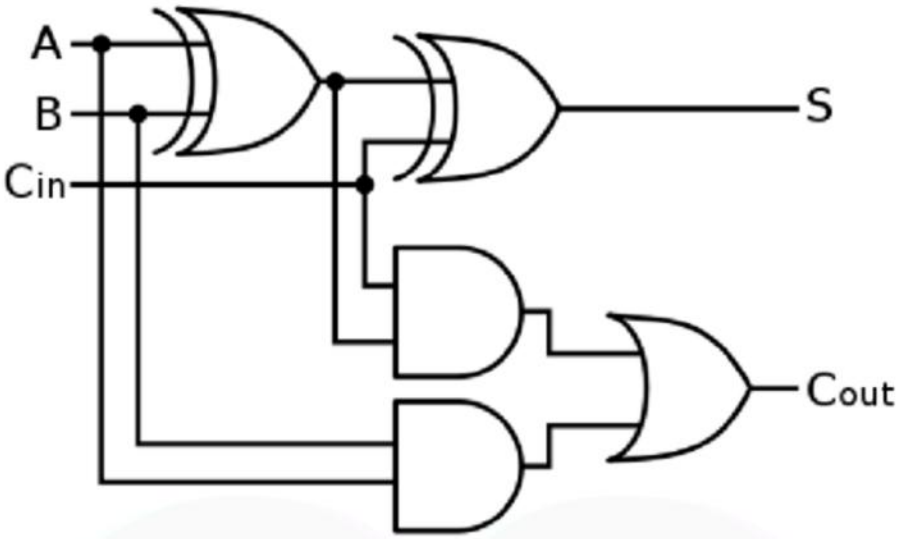
[1]

(b). Draw the output of the flip-flop from Fig. 10.2 on the diagram below.



[3]

6(a). A set of logic gates are connected as below.



(i) Complete the Truth Table below:

A	B	C_{in}	S	C_{out}
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

[4]

(ii) Explain what the circuit does. You should refer to A, B, C_{in}, S and C_{out} in your answer.

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[4]

(b).

(i) Write a Boolean expression equivalent to S.

S ≡

[1]

(ii) Write a Boolean expression equivalent to C_{out}.

C_{out} ≡

[2]

If you found this useful, drop a follow to help me out!

THANK YOU!

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